REMARKS / DISCUSSION OF ISSUES

The present amendment is submitted in response to the Office Action mailed November 24, 2009. In view of the remarks to follow, reconsideration and allowance of this application are respectfully requested.

Status of Claims

Claims 2-10, 16-26 remain in this application. Claims 1 and 7 have been amended. The claims are not believed to be narrowed in scope and no new matter is added.

Allowable Subject Matter

Applicants wish to thank the Examiner for indicating that Claims 3-5, 9, 16-18 and 20-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejections Under 35 U.S.C. §101

Claims 2-10 and 16-26 stand rejected under 35 U.S.C. §101 as being allegedly directed to non-statutory subject matter. As per independent claims 2 and 8, the rejections are understood to be based on the premise that while the claims recite a series of steps or acts to be performed, a statutory process under 35 U.S.C. § 101 must be tied to a particular machine, or transform underlying subject matter to a different state or thing. Claim 2 has been amended in a manner which is believed to obviate the objection. Accordingly, withdrawal of the objection is respectfully requested. Claim 8 recites "means for" language such as distortion means for distorting the bitstream of the primary signal such that the secondary signal is represented by a predetermined distortion, and output means for outputting the bitstream of the primary signal. It is well accepted that for claim limitations invoking 35 USC 112, sixth paragraph, the claim limitations cover the corresponding structure, material, or acts described in the specification and equivalents thereof. See *In re Donaldson*, 29 USPQQ2d 1845 (Fed. Cir. 1994). The distortion means recited in claim 8 covers corresponding structure found at page 7, lines 23-28:

> According to the invention **the hidden channel encoder circuit 54 and the FIFO-buffer 50 are added to a conventional recording apparatus as distortion means** for the creation of the hidden channel. In a format generator for mastering of ROM-discs the clock circuit 53 will generate a clock signal for the encoder circuits and the control of the mastering turn table. In a disc recorder the clock circuit 53 will derive a clock from the format of the disc, e. g. from a groove wobble.

The output means recited in claim 8 covers corresponding structure found at page 7, lines 15-22:

> A provision is taken that the average clock rate of the output clock of the buffer 50 is the same as the input clock provided from the clock circuit 53 to the buffer 50. Further, the buffer 50 should be chosen large enough such that the variations in the output clock rate do not lead to a buffer underrun or overflow. Finally, the primary signal having embedded therein a secondary signal as explained with reference to Figures 1 and 2 is **outputted from the write circuit,** i. e. is written to a record carrier. Alternatively, instead of a write circuit for writing the output signal to a record carrier a transmission circuit could be used for transmitting the output data over a transmission line.

Rejection under 35 USC 103

The Office has rejected claims 2, 6-8, 10 and 19 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,570,339 ("Nagano") in view of U.S. Patent No. 5,546,429 ("Chiason"). Applicants respectfully traverse the rejections.

Claims 2, 6-8, 10 and 19 are allowable

The Office admits that Nagano is silent on the capability of showing wherein distorting the bitstream of the primary signal comprises inserting local phase errors in the bitstream of the primary signal. See Office Action, page 5. The Office attempts to remedy this deficiency by citing Chiason for allegedly teaching this limitation. Specifically, Chiason is cited at col. 7, lines 41-46 for allegedly teaching - - the capability of showing wherein distorting the bitstream of the primary signal comprises inserting local phase errors in the bitstream of the primary signal - -.

Chiason describes a communication unit 100 for a digital communication

system having a transmitter portion 102. The transmitter portion 102 includes data bit coder 108 for encoding a received information signal 106 into a data bit stream 110. The data bit coder 108 preferably encodes the received information signal 106 into a data bit stream 110 according to a information signal coding algorithm and provides the data bit stream 110 to an error control mechanism 112 for subsequent forward error correction encoding, i.e., protecting the data bit stream 110 from transmission errors by convolutionally encoding and interleaving the data bit stream. This protected data bit stream 110 **subsequently has a predetermined synchronization sequence inserted into the error protected data bit stream** such that subsequent maximum ratio diversity combining and maximum-likelihood decoding of the transmitted signal by a hard-limiting receiver 104 is enhanced. See Chiason, col. 7.

The invention relates, in relevant part, to a method of embedding a secondary signal of a secondary channel in the bitstream of a primary signal of a primary channel. However, unlike Chiason, the secondary signal does not constitute **a synchronization sequence** inserted into **an error protected data bit stream** to enhance detection. Rather, the invention is based on the idea to encode a secondary signal of a secondary channel, which may also be called side channel or hidden channel, in a primary signal of a primary channel comprising the original data to be transmitted or to be stored by controlled distortion which distortion may be detected in a Phase Locked Loop (PLL) circuit locked to the primary signal. It should be understood that the invention teaches that the bitstream of the primary signal is **purposefully distorted** before outputting the bitstream of the primary signal such that **the secondary signal of a secondary channel is represented by a predetermined (controlled) distortion.** Unlike Chiason, this secondary signal of the secondary channel does not serve to enhance maximum ratio diversity combining and maximum-likelihood decoding of the transmitted (primary) signal. According to a preferred embodiment of the invention local phase errors are inserted in the bitstream of the primary signal. Thus, at least parts of the stream of lands and marks of the primary signal is displaced with a positive or negative phase error (i.e., the secondary channel). The predetermined or controlled distortion may be detected in a Phase Locked Loop (PLL) circuit locked to the primary signal. More particularly, **the pit and land**

pattern or the mark and space pattern, respectively, of the **primary signal is deliberately distorted by the secondary signal at an encoding stage in a controlled way such that the PLL circuit of a detector can still accommodate for it**. The error signals of the PLL circuit will then contain the information of the secondary signal of the secondary channel.

In further contrast to Chiason, it should be understood that the secondary signal of the invention does not enhance detection, in contrast to the synchronization sequence that is inserted into the primary signal of Chiason. Instead, the local phase errors that constitute the secondary signal of the invention actually slightly spoil the synchronization and therefore force the PLL in the receiver to adjust accordingly.

In light of the above remarks, independent Claim 2 has been amended herein to better define Applicant's invention over Chiason. Claim 2 now recites limitations and/or features which are not disclosed by Chiason. Accordingly, the cited portions of Chiason do not anticipate claim 2, because the cited portions of Chiason fail to disclose every element of claim 2. For example, the cited portions of Chiason fail to disclose or suggest, "*wherein the local phase errors in the bitstream of the primary signal are represented by parts of the stream of lands and marks of the primary signal being displaced relative to an intended nominal position resulting in one of a positive or negative phase error",* as recited in claim 2.

Therefore, the cited portions of the above cited references, individually or in combination, fail to disclose or suggest at least one element of claim 2. Hence, claim 2 is allowable. Claims 6-7 and 19 depend from claim 2, and are therefore allowable at least by virtue of their dependence from allowable claim 2.

Support for the amendment above can be found throughout the specification and in particular -

@ page 2, lines 20-25:

According to a preferred embodiment of the invention local phase errors are inserted in the bitstream of the primary signal. Thus, at least parts of the stream of lands and marks of the primary signal is displaced with a positive or negative phase error which can be detected by the PLL circuit of a detector. Thus, a part of the normal stream of lands and marks is cut out and placed back at slightly shifted position the shift being at maximum half of the channel clock period, preferably 20% to 50% of the channel clock period.

@ page 5, lines 1-11:

Figure 1 shows a channel clock signal 1 and a bit stream 2, i. e. a pit pattern, of a primary signal of a primary channel without a secondary channel over a length L. The normal stream of lands and marks of the primary channel without the secondary channel divided into portions of length L is also shown as a schematic representation 3. According to a first embodiment of the invention local phase errors are introduced into the bitstream 2 of the primary channel. This means that the stream of lands and marks over a length L is displaced with a positive or negative phase error, i. e. a part of the normal stream of lands and marks is cut out and placed back at a slightly shifted position. An example of a primary signal having embedded therein a secondary signal is denoted as 4. Therein the group n+1 (group 41) having a length L is shifted to the right relative to group n introducing a positive shift S, while groups 42 and 43 are shifted to the left introducing negative shifts.

@ page 8, lines 19-25:

If according to the invention a secondary signal is embedded in the primary signal by a predetermined distortion of at least parts of the bitstream of the primary signal as explained above with reference to Figure 1 by use of the additional detector these distortions can be detected and decoded into the secondary signal. If local phase errors are inserted in the bitstream of the primary signal, i. e. if the stream of lands and marks of the primary signal is displaced with a positive or negative phase error, these errors can be detected at the output of the phase detector 631 as indicated by the detector 691.

Independent Claim 8 recites similar subject matter as Independent Claim 2 and therefore contains the limitations of Claim 2. Hence, for at least the same reasons given for Claim 2, Claim 8 is believed to recite statutory subject matter under 35 USC 103(a). Claim 10 depends from claim 8, and are therefore allowable at least by virtue of its dependence from

allowable claim 8.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-7 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Mike Belk, Esq., Intellectual Property Counsel, Philips Electronics North America, at 914-945-6000.

Respectfully submitted,

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